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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,417	03/23/2004	Tetsuya Fukuoka	XA-10058	2265

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
MAI, SON LUU	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,417	FUKUOKA ET AL.	
	Examiner	Art Unit	
	Son L. Mai	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004 and 15 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 7-11* is/are rejected.

7)☒ Claim(s) *4-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed 06/15/04 has been entered. Accordingly claims 1-11 remain pending in the application.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. Figures 7A, 7B and 8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. The disclosure is objected to because of the following informalities:

On page 7, line 17, "off" should be –on--.

On page 15, line 25, "Q17" should be –Q19--.

On page 16, line 1, "Q18" should be –Q20--.

On page 20, line 24, "CN12" should be –CN2--.

On page 21, line 16, "N1" should be –N11--.

In claim 11, line 8, "signal" should be –signals". Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 7-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Abedifard (U.S. Patent 6,560,150).

Regarding claim 1, Abedifard teaches a semiconductor integrated circuit device (figures 1 and 6A) comprising: a latch circuit (502 in figure 6A) coupled to an output (501) of a memory circuit (100), wherein said latch circuit includes a signal selector (606a) for switching between a feedback signal (620) of normal operation mode and a test signal (622) of test operation mode in compliance with an operation mode signal (Sel0) to send out to a feedback loop.

Regarding claim 2, Abedifard teaches a semiconductor integrated circuit device according to claim 1, wherein: said latch circuit (502) is coupled to the output (501) of said memory circuit and, said signal selector (606a) is controlled by said operation mode signal (Sel0) for sending out to said feedback loop either a latch output signal (620) as the feedback signal or an input signal (622) to said memory as the test signal.

Regarding claim 3, Abedifard teaches a semiconductor integrated circuit device according to claim 1, wherein: said latch circuit (502) is coupled to the output (501) of said memory circuit, said signal selector includes a logic gate (606a) for receiving said operation mode signal (Sel0) and latch output signal (620), and said logic gate outputs fixedly an output signal (input signal to pass gate 510) of a predetermined level by the operation mode signal in the test operation mode for sending out to a feedback loop as said test signal.

Regarding claims 7 and 8, Abedifard discloses a semiconductor integrated circuit device (figure 1), comprising a circuit (figure 6A), said circuit operating in either a first mode (normal mode) for operating as a latch; or a second mode (test mode) for passing through a signal input (622) from a signal switching circuit (606a) provided in a feedback loop of said latch (see column 12, lines 12-54).

Regarding claim 9, Abedifard teaches a semiconductor integrated circuit device (figures 1 and 6A), comprising: a first input node (501); a transfer gate (508) coupled to said first input node; an output node (503) coupled to said transfer gate; a feedback loop (signal path through inverter 504, multiplexer 606a, pass gate 510) provided between said first transfer gate and said output node; and a second input node (622) coupled to said feedback loop; said first transfer gate in a first mode (pass gate 508 is turned on) transferring data input from said input node (501) to said output node (503) based on clock signals (RedFireX, RedFireX_n), said first transfer gate (508) in a second mode (pass gate 508 is turned off) disconnecting said input node (501) from

said output node (503); and data being input to said second input node (622) in said second mode (see column 12, lines 20-39).

Regarding claim 10, Abedifard teaches a semiconductor integrated circuit device according to claim 9, wherein: said semiconductor integrated circuit device further comprises a multiplexer (606a in figure 6A) provided in said feedback loop, said multiplexer being coupled to said output node (503) and said second input node (622) to select said output node in said first mode and to select said second input node in said second mode (see column 12, lines 20-39).

Regarding claim 11, Abedifard teaches a semiconductor integrated circuit device according to claim 9, wherein: said semiconductor integrated circuit device further comprises a second transfer gate (510 in figure 6A) provided in said feedback loop, said second transfer gate determining whether or not to feed back the data transferred to said output node based on said clock signals (RedFireX, RedFireX_n) in said first mode, and transferring to said output node (503) the data input to said second input node (622) in said second mode (see column 12, lines 20-39).

Allowable Subject Matter

8. Claims 4-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach or suggest at least the further limitations of claim 5 wherein the latch circuit is coupled to the input of a logic circuit. The latch circuit

includes a first latch for receiving an input signal in the normal operation mode and a second latch for generating a signal input to said logic circuit upon reception of an output from said first latch; and said signal selector is provided in a feedback loop of said first latch.

Conclusion

10. The prior art made of record is considered pertinent to applicant's disclosure. The references cited on form PTO-892 disclose semiconductor integrated circuits comprising a signal selector circuit included in a latch circuit for providing either a normal input signal or a test signal to an output terminal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SON L. MAI
PRIMARY EXAMINER